IN THE CLAIMS:

Please cancel claims 1-16 and 30-43 in their entirety without prejudice nor disclaimer of the subject matter set forth therein.

Please amend claims 17, 18, 49 and 52 as follows.

Claims 1-16. (Cancelled)

17. (Currently Amended) A method for the manufacture of a semiconductor device comprising:

a step of preparing a substrate in which a surface thereof is formed a depression having a triangle or hexagonal figure when viewed from the substrate normal; and

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said depression is filled by said semiconductor layer,

wherein said depression forming step is intentionally performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, n), where said number n is an arbitrary number other than 0, or its equivalent plane.

18. (Currently Amended) A method for the manufacture of a semiconductor device comprising:

a step of preparing a substrate;

a step of forming on a surface of said substrate a depression having a triangle or hexagonal figure when viewed from the substrate normal; and

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said depression is filled by said semiconductor layer,

wherein said depression forming step is intentionally performed such that an inside face of said depression is defined by either a plane having a plane origination of (1, -1, 0, n), where said number n is an arbitrary number other than 0, or its equivalent plane.

19. (Original) The manufacture method of claim 18,

wherein said depression forming step is performed such that an inside face of said depression is defined by either a plane having a plane orientation of (1, -1, 0, 1) or is equivalent plane.

20. (Previously Presented) The manufacture method of claim 19,

wherein said depression forming step is the step of forming on said surface of said substrate defined by a (0, 0, 0, 1) plane a depression having a bottom face whose figure is either an equilateral triangle or an equilateral hexagon.

21. (Original) The manufacture method of claim 17,

wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface.

22. (Original) The manufacture method of claim 21,

wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression.

23. (Original) The manufacture method of claim 18,

wherein said semiconductor layer forming step is the step of forming a semiconductor layer in which an inside face of said depression serves as a crystal growth surface.

24. (Original) The manufacture of claim 23,

wherein said semiconductor layer forming step includes a step in which said semiconductor layer crystal grows in a vertical direction from said inside face of said depression.

25. (Original) The manufacture method of claim 17,

wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor.

26. (Original) The manufacture method of claim 18,

wherein said semiconductor layer forming step is the step of forming a layer which comprises Group III nitride-based compound semiconductor.

27. (Original) The manufacture method of claim 25,

wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method.

28. (Original) The manufacture method of claim 26,

wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method.

29. (Original) The manufacture method of claim 18,

wherein said Group III nitride-based compound semiconductor layer is grown by a metal organic vapor epitaxy method.

Claims 30-43. (Cancelled)

44. (Previously Presented) A method for the manufacture of a semiconductor substrate including:

a step of preparing a substrate for crystal growth;

a step of depositing on said crystal growth substrate a first semiconductor layer having a hexagonal crystal structure;

a step of exposing either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane by subjecting a part of said first semiconductor layer to an etching process; and

after said exposing step, a step of depositing on said first semiconductor layer a second semiconductor layer having a hexagonal crystal structure, whereby said plane is covered with said second semiconductor layer.

45. (Previously Presented) The manufacture method of claim 44,

wherein said exposing step includes:

a step of applying onto said first semiconductor layer a resist pattern having an opening whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and

a step of forming a depression by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said depression has an inside face comprising either a plane having a plane orientation of (1, -1, 0, n) where said number n is an arbitrary number, or its equivalent plane.

46. (Original) The manufacture method of claim 45,

wherein said resist pattern has a plurality of said openings arrayed at equal intervals.

47. (Previously Presented) The manufacture method of claim 44,

wherein said exposing step includes:

a step of applying onto said first semiconductor layer a resist pattern whose figure is either substantially an equilateral triangle, or substantially an equilateral hexagon when viewed from the substrate normal; and

a step of forming a projection by subjecting said first semiconductor layer to an etching process in which said resist pattern is used as a mask so that said projection has a side face comprising either a plane having a plane orientation of (1, -1, ,0, n) where said number n is an arbitrary number or its equivalent plane.

48. (Original) The manufacture method of claim 47,

wherein said resist pattern comprises a plurality of said resist patterns arrayed at equal intervals.

49. (Currently Amended) A method for the manufacture of a semiconductor substrate comprising:

a step of forming a substrate having on a surface thereof a depression having a triangle or hexagonal figure when viewed from the substrate normal;

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said structure is filled by said semiconductor layer; and

a step of taking out said semiconductor layer by removal of said substrate,

wherein said depression has an inside face intentionally defined by either a plane having a plane orientation of (1, -1, 0, n), where said number n is an arbitrary number other than 0, or its equivalent plane.

50. (Original) The manufacture method of claim 49,

wherein said depression has an inside face defined by either a plane having a plane orientation of (1, -1, 0, 1) or its equivalent plane.

51. (Original) The manufacture method of claim 50,

wherein said depression has in major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon.

52. (Currently Amended) A method for the manufacture of a semiconductor substrate comprising:

a step of forming a substrate having on a surface thereof a triangle or hexagonal projection;

a step of forming on said surface of said substrate a semiconductor layer having a hexagonal crystal structure, whereby said projection is capped with said semiconductor layer; and

a step of taking out said semiconductor layer by removal of said substrate,

wherein said projection has a side face intentionally defined by either a plane having a plane orientation of (1, -1, 0, n), wherein said number n is an arbitrary number other than 0, or its equivalent plane.

53. (Original) The manufacture method of claim 52,

wherein said projection has a side face defined by either a plane having a plane orientation of (1, -1, 0, 1) or is equivalent plane.

54. (Original) The manufacture method of claim 52,

wherein said projection has, in said major surface of said substrate defined by a (0, 0, 0, 1) plane, a bottom face whose figure is either an equilateral triangle or an equilateral hexagon.

55. (Original) The manufacture method of claim 49,

wherein said semiconductor layer forming step is the step of forming a layer of Group III nitride-based compound semiconductor.

56. (Original) The manufacture method of claim 52,

wherein said semiconductor layer forming step is the step of forming a layer of group III nitride-based compound semiconductor.

57. (Original) The manufacture method of claim 55,

wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy.

58. (Original) The manufacture method of claim 56,

wherein said Group III nitride-based compound semiconductor layer is grown by hydride vapor phase epitaxy.

59. (Original) The manufacture method of claim 49,

said substrate forming step including:

a step of preparing a sapphire substrate; and

a step of forming on said sapphire substrate a group III nitride-based compound semiconductor layer having said depression in a surface thereon.

60. (Original) The manufacture method of claim 52,

said substrate forming step including:

a step of preparing a sapphire substrate; and

a step of forming on said sapphire substrate a group III nitride-based compound semiconductor layer having said projection on a surface thereof.